REMARKS

Claims 2 and 14 are amended herein. Claims 1-14 and 18, 19, 21 and 22 remain pending in the application.

In the Drawings

Fig. 2 was objected to as allegedly mislabeling drain-source voltage of switch MC in Fig. 1.

Applicant proposes to change Fig. 2 to match the description in the Specification. No new matter is added. It is respectfully requested that the proposed changes be approved and that the objection to the Drawings be withdrawn.

Objection to the Disclosure

The disclosure was again objected to for an alleged informality. In particular, the Examiner alleges that switch MC, described at page 7, line 18 of the disclosure should be labeled switch MS. The Examiner questions why MC is identified as a switch on lines 18 and 19, but as a current source on line 21.

A reading of the entire paragraph, page 7, lines 17-22, shows the labels of the referenced switches is correct. The Applicant is describing using the mirror path to equalize the current level on both sides of the current source switch MC. The switch MC is a switched current source.

Moreover, the Examiner questions how the Applicant equalizes something that is already equal, or substantially equal? In particular, the Examiner alleges that since current flowing through switch (transistor) MC will have minimal loss due to leakage current within the transistor, the current level at the source of MC is considered equal to the current level at its drain (Office Action, page 13).

As Applicant has repeatedly tried to convey to the Examiner, charge injection is a current spike associated with switching of a capacitive current source. When a current source enters its saturation from a triod state, minority carriers from an inversion layer of the current source may be injected into a load capacitor (Specification, page 2, lines 1-11).

Withdrawal of the objection is respectfully requested.

Section 112 rejection of Claims 1-14, 18, 19, 21 and 22

Claims 1-14, 18, 19, 21 and 22 were rejected under 35 USC 112, second paragraph. The Applicant respectfully traverses the rejection.

Claims 1, 18, 21 and 22

Claims 1, 18, 21 and 22 allegedly claim unclear language, i.e., "to equalize a current level produced by said current source". The Applicant is describing using a mirror path to equalize current levels on both sides of a current source, e.g., page 7, lines 17-22 of the Specification.

The Examiner questions what the current source is equalized with respect to (Office Action, page 17). The current source is equalized with respect to itself. A current source that is equalized has its own variations eliminated.

The Examiner questions that if the current source is providing a constant current, wouldn't that be considered equal to its desired operational current. Equalization does not simply mean operating a current source at its desired operational current, although that could possibly be the ultimate result of equalization. As discussed above, equalizing a current level produced by a current source eliminates variations within the current source, as described in the Specification at, e.g., page 7, lines 17-22.

Claims 1, 2 and 14

Claims 1, 2 and 14 allegedly unclearly claim "a current source".

Claims 2 and 14 have been reviewed and are amended where appropriate to clear up antecedent basis. It is respectfully submitted that the claims are now in full conformance with 35 USC 112. It is respectfully requested that the rejection be withdrawn.

Claims 21 and 22

The Office Action **again** alleges that the language "continuously receives said current flowing from said current source" is still misleading from claims 21 and 22. The Applicant respectfully disagrees.

A reading of the entire claim language indicates the limitation reads "**substantially** continuously receives said current flowing from said current

source". The mirror path diverts the charge injection to ground when the switch at the current source is initially opened. Therefore, the load substantially continuously receives current since the charge injection only exists for a **very short time** when current switch initially allows current to flow to a load. The Examiner is ignoring the claim limitation as a **whole**. The Applicant is **NOT** claiming a load that "continuously" receives current, as the Examiner alleges, but is claiming a load that "**substantially continuously**" receives current.

The Examiner questions when the load substantially continuously receives current since the charge injection only exists for a very short time when the current switch initially allows current to flow to a load, is the current from the current source, or is it provided from the voltage stored across capacitor C1? (Office Action, page 14).

The Applicants are claiming the invention broadly, as a current source. As the claims stand, the claims are clearly written as broadly claiming a current source. The invention is clearly disclosed in that the current source, e.g., current source MC and current source 420, are the current sources of the circuit.

The Examiner is requested to consider the claim language as a whole, and not as parts taken out of context.

Any claims not specifically addressed under 35 USC 112, second paragraph above are rejected based on dependency.

All the claims are in full conformance with 35 USC 112, and the Applicant requests the rejections be withdrawn.

Claims 1-5, 8-10, 12-19, 21 and 22 over Ravon

In the Office Action, claims 1-5, 8-10, 12, 18, 19, 21 and 22 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by US Patent No. 6,137,275 to Ravon ("Ravon"), and claims 13 and 14 are rejected as obvious over Ravon. The Applicant respectfully traverses the rejection as follows.

Claims 1-5, 8-10, 12, 18, 19, 21 and 22 recite, *inter alia,* reduction of charge injection.

Ravon appears to teach a system for providing a regulated voltage meant to supply a load (Ravon, Abstract). A current source providing the

maximum current likely to be surged by the load, and a device for receiving the constant current and regulating the load supply voltage (Ravon, Abstract). A source 11 provides a constant voltage to a load, within a maximum current value that the load is likely to consume (Ravon, col. 3, lines 35-43). A regulating device 10 eliminates transients of the voltage supply to a load (Ravon, col. 3, lines 24-34). The regulating device includes a MOS power transistor M1, a MOS transistor M2, a transistor bias control circuit 13, and a comparator 14 (Ravon, Fig. 2; col. 3, line 49-col. 5, line 18). Transistor M2 controls the flow of current from the current source to ground (Ravon, Fig. 2). Transistor M1 controls the flow of current from the current source to the load (Ravon, Fig. 2).

Ravon's system is designed to supply a regulated voltage, at varying currents but within a maximum surge current (Ravon, col. 3, lines 35-44). The duel paths within Ravon's item 10 operate to limit transient variations of voltage Vout supplying a load, e.g., a microprocessor (Ravon, col. 3, lines 24-27). Ravon supplies an uninterrupted voltage and current supply. Elimination of voltage transients is NOT reduction of charge injection, as claimed by claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22.

The Office Action alleges Harton's duel paths operate to reduce charge injection (Office Action, pages 5). The Applicant respectfully disagrees.

Charge injection relates to the current spike that occurs most frequently during a switch state of either a MOS transistor switch or, more seriously, when a current source enters its saturation from a triod state, minority carriers from the inversion layer of the current source may be injected into the load. Ravon teaches the purpose of MOS transistor M2 is to absorb excess current during periods when the load only requires a low supply current. Ravon's **uninterrupted** current source is not taught as even being capacitive, and producing current spikes during **switching**. Ravon's **load** is creating the current fluctuations. **Loads do not create charge injection**. Reducing excess current during periods when the load only requires a low supply current (col. 3, lines 59-62) is **NOT** charge injection, as claimed by claims 1-5, 8-10, 12-14, 18, 19, 21 and 22.

Claims 1-5, 8-10, 12-14, 18, 19, 21 and 22 recite, *inter alia,* a pull-down mirror path in parallel with a transistor switch operating to equalize the current level produced by a current source.

Ravon fails to even mention the duel paths operating to equalize the current level produced by a current source. A method for two paths to equalize the current level produced by a current source is, e.g., each path having a matched impedance. Since current is a function of impedance, if each path has equal impedance, the current level produced by the current source would remain constant no matter which path is conducting current. Ravon fails to teach a pull-down mirror path in parallel with a transistor switch operating to equalize the current level produced by a current source, as claimed by claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22.

The Examiner argues that clarification is still required as to how current from a current source can flow to a load when a switching transistor is open, as recited within the claims (Office Action, page 15). In particular, the Examiner alleges the current associated with resistor R1 and capacitor C1 is not the current IA from the current source as claims 21 and 22 clearly recite (Office Action, page 15).

Nowhere in either of claims 21 and 22 does Applicant claim "resistor R1" or "capacitor C1", much less a current associated with resistor R1 and capacitor C1 being the same as a current IA from a current source as allegedly claimed by claims 21 and 22. The Examiner is incorrectly reading limitations from the specification into the claims.

Moreover, the Examiner alleges that the previous amendment's comments, the specification, and the figures do not show, or clearly disclose, how current flows to ground through the pull-down mirror path. **NOWHERE**, not in the previous amendment, not in the specification, or in any figure does Applicant disclose current flows to ground through the pull-down mirror path. The Applicant discloses a pull-down mirror path that is connected to ground. The pull-down mirror path is used to reduce charge injection.

The Examiner alleges the Applicant is attacking the references individually, where the rejections are based on combinations of references

(Office Action, page 17). The Examiner rejects claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22 over Ravon individually. The Examiner alleges the references don't have to specifically teach reducing charge injection by a pull-down mirror path (Office Action, page 17). The Applicant respectfully disagrees.

The Examiner rejected claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22 as being anticipated by Ravon. Therefore, Ravon **MUST** teach reducing charge injection by a pull-down mirror path, as claimed by claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22.

The Examiner alleges that he believes the Applicant's current source is not switched (Office Action, page 16).

The Examiner is correct that the Applicant is not claiming a switching current source. The Applicant discloses in the specification that charge injection is a result of, e.g., a switching current source or a switch receiving charge injection from a load capacitor (Specification, page 2, lines 1-11). Claiming simply a "current source" allows the Applicant to claim the invention broadly without specifying what the current source is as the source of charge injection. Therefore, any current source that is associated with charge injection would be covered by Applicant's claimed invention.

Accordingly, for at least all the above reasons, claims 1-5, 8-10 and 12-14, 18, 19, 21 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 6, 7 and 11 over Ravon in view of AAPA

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Ravon in view of Applicant's Admitted Prior Art Fig. 3 (AAPA). The Applicant respectfully traverses the rejection as follows.

Claims 6, 7 and 11 are dependent on claim 1, and are allowable for at least the same reasons as claim 1 is allowable.

Claims 6, 7 and 11 recite, *inter alia,* reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

As discussed above, Ravon fails to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

The Office Action correctly acknowledged that Ravon fails to teach a serial combination of transistors. The Office Action relies on AAPA to make up for the deficiencies in Ravon to arrive at the claimed invention. The Applicant respectfully disagress.

AAPA teaches an unsatisfactory circuit for reducing charge injection which uses a serial combination of transistors forming a compensating switch (AAPA, Fig. 3). AAPA fails to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize the current level produced by a current source, as claimed by claims 6, 7 and 11.

AAPA and Ravon fail to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize the current level produced by a current source, as claimed by claims 6, 7 and 11.

Accordingly, for at least all the above reasons, claims 6, 7 and 11 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-5, 8-10, 12-14, 18 and 19 in view of Harston

In the Office Action, claims 1-5, 8-10, 12-14, 18 and 19 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over US Patent No. 5,343,196 to Harston ("Harston"). The Applicant respectfully traverses the rejection as follows.

Claims 1-5, 8-10, 12-14, 18 and 19 of the present application recite, *inter alia,* reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

Harston teaches a method of reducing the amount of current switched to a reference line so as to reduce the overall power consumption of a digital to analog converter (DAC). To achieve this, three transistors are employed. One MOS transistor acts as a current source. The two other

transistors act alternatively to direct current to either a load or alternately to ground (Harston, col. 1, line 41-42). The current directed to ground performs no useful purpose (Harston, col. 1, lines 20-23).

Harston alternate path to ground performs no useful purpose. Harston alternate path to ground does not reduce charge injection, as claimed by claims 1-5, 8-10, 12-14, 18 and 19.

Claims 1-5, 8-10, 12-14, 18 and 19 recite, *inter alia*, a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

Harston is unconcerned with equalizing the current level produced by a current source. Harston simply changes the state of a DAC as either receiving current from a source or not receiving current from a source.

Harston fails to teach a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source, as claimed by claims 1-5, 8-10, 12-14, 18 and 19.

The Office Action argues that Harston's current cell could be called a current source switching circuit and could be used in other circuits, besides a DAC, that would require switched current when necessary (Office Action, page 19).

Placing Harston's current cell in other circuits does not overcome the fact the Harston's alternate current path is used to switch current away from a DAC. Current is switched away from the DAC to prevent the DAC from being powered, NOT because of charge injection. Harston's current remains constant, as the Examiner acknowledges (Office Action, page 20), and would not produce charge injection from switching associated with a capacitive current source.

Accordingly, for at least all the above reasons, claims 1-5, 8-10, 12-14, 18 and 19 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 6, 7 and 11 over Harston in view of AAPA

In the Office Action, claims 6, 7 and 11 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Harston in view of AAPA. The Applicant respectfully traverses the rejection as follows.

Claims 6, 7 and 11 are dependent on claim 1, and are allowable for at least the same reasons as claim 1 is allowable.

Claims 6, 7 and 11 of the present application recite, *inter alia,* reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

As discussed above, Harston fails to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source.

As discussed above, AAPA fails to teach a transistor switch and a pull-down mirror path that operate to substantially continuously reduce charge injection flowing to a load.

Harston and AAPA fails to teach reduction of charge injection by a pull-down mirror path in parallel with a transistor switch operating to equalize a current level produced by a current source, as claimed by claims 6, 7 and 11.

Accordingly, for at least all the above reasons, claims 6, 7 and 11 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

The Examiner appears to maintain that the purpose of the cited references is to reduce the amount of current to a load or reduce variations in current, which equates to the claimed charge injection (Office Action, pages 15 and 16). The Applicant respectfully disagrees.

The Applicant's invention redirects a current spike produced by a capacitive current source to mirror path. Current spikes produced by a capacitive current source are released at the time the current source is switched on. Neither of the cited references recite a reduction of charge injection. The

references reduce current, **not** charge injection as in the present invention. The Examiner is reading features into the references that simply are not taught by the cited prior art.

The Examiner alleges that although the prior art fails to specifically use the terminology of reducing charge injection, the cited prior art teaches a reduction of charge injection inherently from their operation (Office Action, page 18). As discussed above, the cited prior art fails to mention reducing charge injection because the cited prior art fails to teach reducing charge injection.

Charge injection is a term of art relating to current spikes associated with switching of a capacitive current source or a capacitive load (Specification, page 2, lines 1-11). Current is switched to an alternate path, i.e., a pull-down mirror path, at the time of switching to eliminate current spikes. None of the prior art teaches elimination of charge injection, i.e., current spikes associated with switching of either a capacitve current source or a capacitve load.

The Examiner supports the fact the prior art fails to teach reducing charge injection by citing prior art that contains current sources which "**continuously** provide current" to one of two selected current paths (Office Action, page 20). "**None**" of the current sources appear to be turned on and off during normal operation, and thus would "not provide associated spikes" related to their switching (Office Action, page 20).

None of the cited prior art teaches reducing charge injection because, as the Examiner admits, the cited prior art is unconcerned with switching, much less that current spikes associated with switching. No switching equates to no charge injection.

All rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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Version with Markings to Show Changes Made

2. (Amended) The current source switching circuit according to claim 1, [further comprising] wherein:

[a] said current source is connected between a power source and a first side of said transistor switch.

14. (Amended) The current source switching circuit according to claim 13, [further comprising] wherein:

[a] said current source is connected between a ground and a first side of said transistor switch.